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5,188,976 ("Kume") in view of Tada, U.S. Patent No. 5,497,021 ("Tada"). Applicants respectfully traverse these rejections.

I. Response to Rejections under 35 U.S.C. § 112, first paragraph

In this rejection, the Examiner maintained the reasons presented in the Office Action dated June 6, 2002. Further, in response to Applicants' arguments advanced in the Response filed September 4, 2002, the Examiner alleged that Applicants' response does not deal with the issue of the rejection. Specifically, the Examiner stated that "the rejection deals with the lack of an insulation layer between the gate and the semi conducting substrate" (FOA, p. 3). In response, Applicants assert that the Examiner's allegations and grounds for rejection are improper.

A rejection under 35 U.S.C. § 112, first paragraph, involves an analysis of whether a particular claim is supported by the disclosure. This analysis requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. *See* M.P.E.P. § 2164.01 (Aug. 2001 8th Ed.), p. 2100-174.

As advanced in the September 4th response, the specification illustrates and describes two transistors which are connected by a side wall as recited in the claims. For example, Figures 10, 13A-D, and 20B (related text on pages 32-38, 45, and 46) illustrate and describe two transistors which are connected by a side wall. Furthermore, the Examiner fails to clearly address why the specification does not enable the claimed invention. In the rejection and response to Applicants' arguments, the Examiner merely addressed the subject matter recited in the claims, but does not establish a factual basis to support his allegation that the specification lacks an enabling disclosure (or the subject matter). Thus, the rejection under 35 U.S.C. § 112, first paragraph, is improper. Accordingly, Applicants request that the Examiner withdraw this rejection.

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In making the various references to the specification and drawings set forth above, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

II. Response to Rejections under 35 U.S.C. § 112, second paragraph

In this rejection, the Examiner maintained the reasons presented in the Office Action dated June 6, 2002. Further, in response to Applicants' arguments advanced in the response filed September 4th, the Examiner alleged that Applicants' response does not deal with the issue of the rejection. More particularly, the Examiner alleged that the rejection is not based on ambiguity of sidewall location but ambiguity in which channel direction Applicant claims (FOA, p. 3). In response, Applicants assert that the Examiner's rejection is improper.

As advanced in the September 4th response, the claims clearly recite the location of the sidewalls. Specifically, claim 27 recites "wherein a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction." Thus, the channel direction as claimed defines the location of the sidewalls. Thus, Applicants submit that the Examiner's rejection under 35 U.S.C. § 112, second paragraph, is improper. Accordingly, Applicants request that the Examiner withdraw this rejection.

III. Response to Rejection under 35 U.S.C. § 103(a)

In this rejection, the Examiner maintained the reasons presented in the June 6th Office Action. In response, Applicants assert that a *prima facie* case of obviousness has not been established because Kume and Tada, taken alone or in combination, fail to teach or suggest all the claim elements and there is no motivation to combine the references.

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In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Furthermore, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *See* M.P.E.P. § 2143.01 (8th Ed., Aug. 2001), *quoting In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. *See* M.P.E.P. § 2143 (8th Ed. 2001), pp. 2100-122 to 127.

Claim 27 is directed to a semiconductor device comprising a combination of elements including, *inter alia*, "a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction."

In rejecting claim 27, the Examiner maintained the reasons presented in the June 6th Office Action. Specifically, the Examiner alleged that Kume describes all the elements of claim 27 except for a side wall of the first gate electrode at one end of a channel direction being connected to a side wall of the second gate electrode at one end of the channel direction, and alleged that Tada teaches this claim element (Office Action, p. 5). In the September 4th Response, Applicants pointed out that Tada does not teach or suggest at least that "a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction." In response to Applicants' arguments, the Examiner alleged that Tada, in Fig. 3d, illustrates an element 21 connecting gate electrodes sidewalls 13a and 13b (FOA, p. 4). Applicants respectfully submit that the Examiner has misconstrued Tada.

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Tada, Fig. 3d, illustrates "[a] step cross sectional [view] showing a part of a production process of the semiconductor device shown in Fig. 1." Tada, col. 4, lines 50-52 (emphasis added). Fig. 3d, however, does not even illustrate gate electrodes 13a and 13b. Fig. 3d only illustrates polysilicon layer 23 which is patterned to form gate electrodes 13a and 13b. Tada, col. 7, lines 10-14. Tada, Fig. 1, illustrates the complete constructed semiconductor device. However, Tada, Fig. 1, fails to disclose that the sidewalls of gate electrodes 13a and 13b are connected. *See* Tada, col. 8, lines 1-11. Thus, contrary to the Examiner's allegations, Tada fails to teach or suggest at least, "a side wall of said first gate electrode at one end of a channel direction is connected to a side wall of said second gate electrode at one end of the channel direction," as recited in claim 27. Thus, a *prima facie* case of obviousness has not been established for claim 27 (Kume also fails to teach or suggest this claim element, *See* September 4th Response for a complete discussion). Accordingly, for at least this reason, claim 27 is allowable.

Furthermore, there is no suggestion or motivation to modify Kume with Tada (or vice versa) to produce Applicants' claimed invention. The Examiner alleged that "it would have been obvious ... to include Tada's direct connection between gate electrodes 13 a and b ... in Kume's device to reduce the device size." (Final Office Action, p. 4 referencing previous Office Action dated June 6, 2002). First, as advanced above, Tada fails to teach or suggest that gate electrodes 13a and 13b are connected. Thus, the Examiner's reasoning is incorrect for at least this reason.

Second, even if the Examiner's allegations that "it would have been obvious... to include Tada's direct connection ... in Kume's device" (Final Office Action, p. 4 referencing previous Office Action dated June 6, 2002), were true (which Applicants dispute), this still does not establish that there would have been the requisite suggestion or motivation to modify either

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Kume or Tada to produce Applicants' claimed invention. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01, p. 2100-124, *citing In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (emphasis in original).

Since Kume and Tada, taken alone or in combination, do not teach or suggest all the recitations of Applicants' claimed invention, and there can be no suggestion or motivation *in the cited references* to modify them, Applicants submit that the cited references do not suggest the desirability of their modification to produce Applicants' present invention.

Thus, a *prima facie* case of obviousness has not been established for claim 27. Accordingly, for at least this reason, claim 27 is allowable.

Claims 28 and 30-33 are allowable at least due to their dependence from allowable claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." M.P.E.P. § 2143.03, p. 2100-126 *citing In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

In the Advisory Action dated March 10, 2003, the Examiner alleged that Applicants' arguments presented in the Request for Reconsideration filed February 10, 2003 were not persuasive. Particularly, the Examiner alleged that Tada, Fig. 3d, illustrates the final structure obtained by steps in Figs. 3a-3d, which is a different embodiment from that described in Fig. 1 of Tada and that Fig. 3d illustrates gate electrodes 13a and 13b. (Advisory Action, p. 2). Contrary to the Examiner's allegation, Tada explicitly recites that Fig. 3d, illustrates "[a] step cross sectional [view] showing a part of a production process of the semiconductor device shown in Fig. 1." Tada, col. 4, lines 50-52 (emphasis added).

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Moreover, the Examiner's allegation that Fig. 3d illustrates gate electrodes 13a and 13b is incorrect. Attached is Exhibit A which is an enlarged copy of Tada Fig. 3d. As seen in Exhibit A, a layer of polycrystalline silicon layer 23 and 13 is formed on the entire structure of device 1. This layer contacts every element of device 1. In fact, Fig. 3d fails to illustrate the steps performed to create electrodes 13a and 13b. Specifically, Tada teaches that

> Then, on the surface side of the second polycrystalline silicon layer 23 is formed a resist mask layer. Then after patterning, dry etching and removing the resist layer, polycrystalline silicon layers 23a and 23b (gate electrodes 13a and 13b) are left only in a desired region of the low voltage drive circuit portion 1a. Tada, col. 7, lines 10-15.

In other words, gate electrodes 13a and 13b are not formed until a step subsequent to the process step illustrated in Fig. 3d. This subsequent step is performed between the unfinished device illustrated in Fig. 3d and the device illustrated in Fig. 1. Gate electrodes 13a and 13b are only illustrated in Fig. 1. Attached is Exhibit B which is an enlarged copy of Tada Fig. 1. As shown in Exhibit A, Tada discloses that the sidewalls of gate electrodes 13a and 13b are not connected.

Additionally, the Examiner cited col. 8, line 1, of Tada to support his argument that Fig. 3d illustrates gate electrodes 13a and 13b. (Advisory Action, p. 2) However, this citation supports our position since the cited text is describing the semiconductor device illustrated in Fig. 1. *See* Tada, col. 7 line 36 to col. 8, line 2. Thus, the Examiner's arguments presented in the November 11th Final Office Action and March 10th Advisory Action are incorrect.

Conclusion

In view of the foregoing, Applicants respectfully request the reconsideration and reexamination of this application and the timely allowance of the pending claims.

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: April 8, 2003

By: _____

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EXHIBIT A

FIG. 3(d)

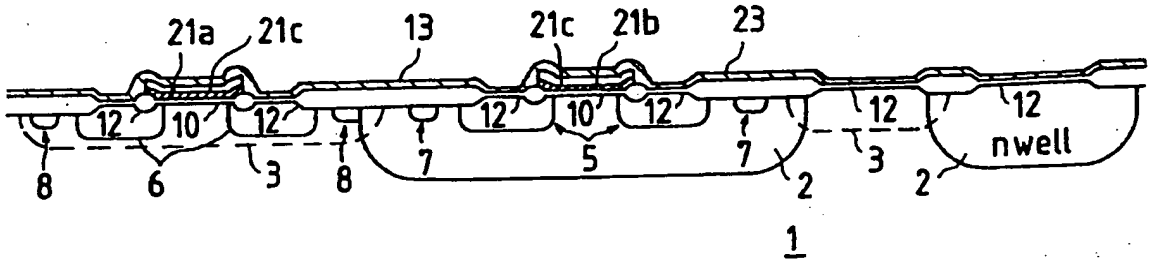

EXHIBIT B

FIG. 1